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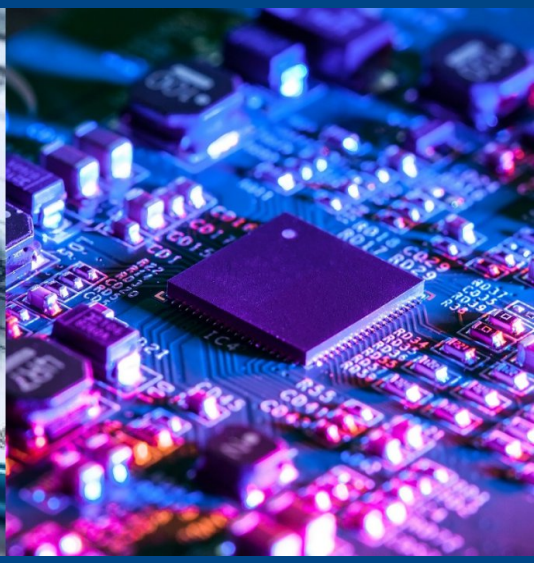

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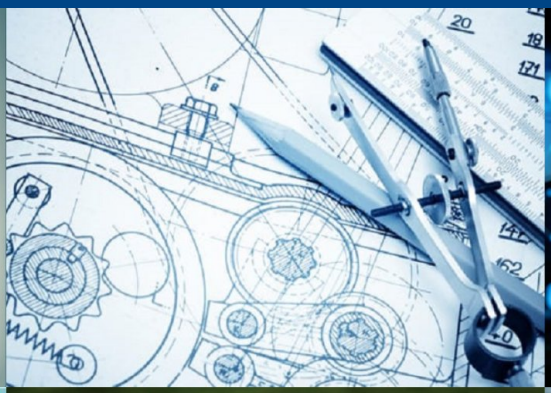

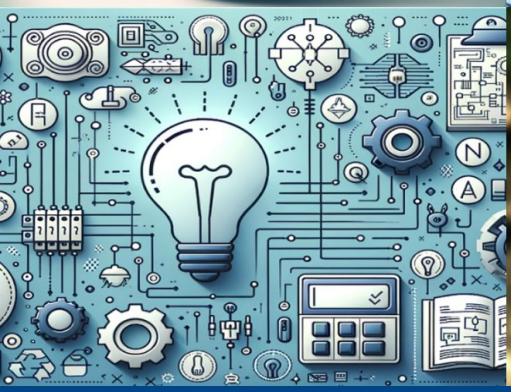

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Wireless Sensor Network Fault Detection using a Random Forest Classifier Implementing on FPGA

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ABSTRACT: Fault detection in Wireless Sensor Networks are indispensable in maintaining reliable conveyance and network performance. Techniques often rely on manual diagnosis or single model approaches, which suffer from lower accuracy and delayed responses, especially in large-scale or real-time sensor environments. These limitations can lead to undetected node failures, data loss, and increased maintenance costs. To overcome these challenges, this work presents a composite Machine Learning–based Fault Detection System that integrates the predictive capabilities of Random Forest (RF), Support Vector Machine (SVM), and XGBoost (XGB) models. The hybrid ensemble effectively analyses sensor and network parameters such as battery level, temperature, humidity, signal strength, and packet loss rate to detect abnormal node behaviour with high accuracy. Once a fault is detected, classification result is transmitted to an FPGA module (XC9572XL), which controls visual alerts using ON/OFF indicator LED to signify node health status. Additionally, an ESP32 microcontroller integrated to communicate between fault status for remote monitoring and alert generation. The proposed system achieves improved accuracy and real-time alerting capability compared to conventional models. By combining intelligent software prediction with hardware-level indication, the system enhances network reliability, supports early fault diagnosis, and enables efficient maintenance in WSN environments. SHAP-based feature importance analysis is employed to identify the most influential parameters contributing to fault prediction. To analyze key sensor and network parameters such as battery level, signal strength, temperature, humidity, and packet loss rate for identifying abnormal node behaviour. To implement the detected fault status on an FPGA (XC9572XL) for hardware-based visual indication through LED signalling. To integrate the ESP32 module for real-time transmission of fault alerts and system status to external monitoring interfaces management, paving the way for smarter, more self-reliant sensor networks capable of adapting to complex and dynamic environments.

KEYWORDS: WSN, FPGA, fault diagnosis, random forest classifier

I. INTRODUCTION

Wireless Sensor Networks (WSNs) represent a rapidly evolving domain within the field of embedded systems and intelligent communication technologies. A WSN consists of a collection of spatially distributed sensor nodes that monitor and record environmental, physical conditions such as temperature, humidity, pressure, air quality, vibration, and more. These nodes communicate wirelessly to transmit the collected data to a central system or base accurate fault identification and immediate alert generation. Software specifications include Windows 10Operating system, Python (IDLE), Streamlit. Hardware specifications are ESP32, FPGA XC9572XL. Processing modules include Data Acquisition, Preprocessing, Data Splitting, Hybrid Machine Learning Model Building, Hybrid Model Training and Evaluation, Streamlit Web Application, Hardware Alert and Communication. Python programming language is used for this task. Scikit-learn the most popular ML libraries used in this project for classical ML algorithms. Streamlit is ideal for: Building data dashboards station for analysis and decision-making. In recent years, WSNs have or exploratory data analysis (EDA) tools, creating interactive become integral to industrial automation, environmental monitoring, smart cities, healthcare systems, precision agriculture, and defense simulations or apps for teaching and presentations. Streamlit provides an easy and fast way to turn Python scripts into interactive web apps. The surveillance. Their ability to provide real-time sensing and ESP32 (30-pin) development board a popular microcontroller based on communication makes it essential for data-driven decision processes in modern IoT and cyber-physical systems. However, the reliability of WSNs is often challenged by node failures, communication faults, and environmental interferences. Factors such as limited battery life, signal loss, temperature fluctuations, and hardware malfunctions can lead to inaccurate readings or complete node failure, ultimately affecting the overall

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performance of the network. To overcome this, machine learning and intelligent fault prediction models have become crucial in ensuring the stability and resilience of WSNs. By analyzing l sensor data and identifying fault patterns, these models can predict and classify faulty nodes before they disrupt network operations. The integration of Hybrid Machine Learning approaches with hardware- based alert mechanisms enhances system dependability by combining intelligent analytics with real-time fault indication. The fusion of data science and embedded systems marks a significant advancement in the domain of WSN. The process begins by connecting a JTAG programming tool (such as the Xilinx Platform Cable USB or the Digilent JTAG programmer) to the JTAG header on the Xilinx device. The programmer interfaces with the JTAG chain, which may include multiple devices, allowing them to be programmed sequentially or in parallel. The JTAG port is connected to a host computer running Xilinx's development tools like Vivado or ISE (Integrated Software Environment).

II. EXPERIMENTAL DETAILS

The system integrates both software- and hardware-based solutions for the ESP32-WROOM 32 module. Below are the details of its 30 pins, including power, GPIO, ADC, DAC, PWM, I2C, SPI, UART, and special function pins has been used. Using FPGA XC9572XL hardware, the board can be easily programmed using the Xilinx ISE Design Suite software through a USB JTAG cable, which loads ajed (JEDEC) configuration file into the CPLD. This project aims to develop a Hybrid Machine Learning–based fault detection model integrated with FPGA (XC9572XL) for real-time LED indication and ESP32 for wireless alert communication, ensuring reliable and responsive fault management in WSN environments. Once a fault is detected, the result is transmitted to the FPGA module (XC9572XL), which controls an LED indication system—turning ON or OFF based on the fault condition. This integration ensures a seamless flow from intelligent fault prediction to real-time hardware alerting, thereby enhancing the reliability and maintainability.

III. IMPLEMENTATION

The proposed System is structured into seven main modules. Data Acquisition is responsible for collecting environmental and network- related parameters from sensor nodes deployed in the WSN. Data Preprocessing ensures consistency of data. Duplicate entries are removed, and categorical features are converted into numerical format using Label Encoding. In Data Splitting, processed dataset is indoctrinated as (80:20). Hybrid Machine Learning Building imparts to the finalization. RF offers robustness and feature selection, SVM provides strong classification boundaries, and XGB enhances learning efficiency through boosting. Hybrid Model Training and Evaluation enables to learn the relationships between sensor readings and fault occurrences. During testing, the model predicts operational status (Normal or Faulty) of each node. Users can upload WSN test dataset in CSV format, initiate prediction sand instantly view the classification results, confidence scores and visual charts. Hardware integration ensures detected faults are immediately communicated through physical signals, enabling faster response and action maintenance. Feature importance analysis from the Random Forest model highlights the most influential parameters contributing to fault detection in the wireless sensor network. XC9572XL includes a clock distribution network that ensures proper timing and synchronization of the logic elements, preventing setup and hold time violations. XC9572XL consists of programmable logic blocks (PLBs), which allow for the creation of custom digital logic circuits.

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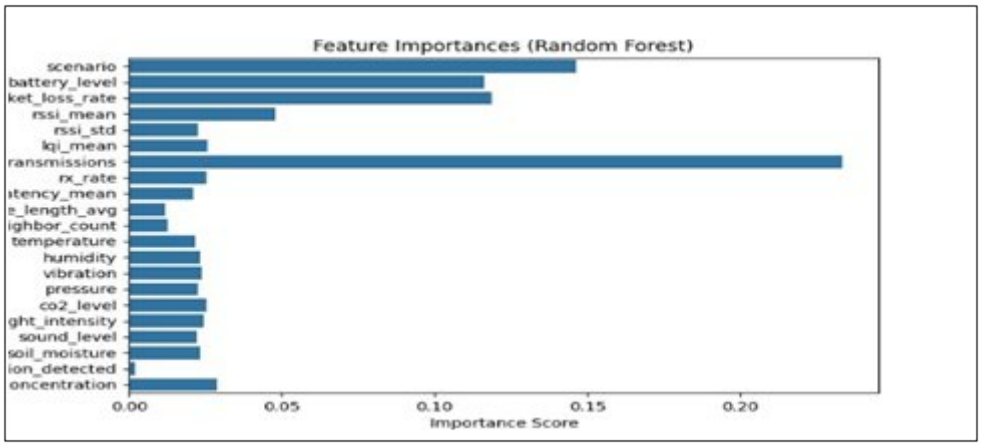

FIGURE.1. FEATURE IMPORTANCE

Among all features, transmissions, scenario, and battery level exhibit the highest importance scores, indicating that communication activity, network context, and energy status play crucial roles in determining network faults.

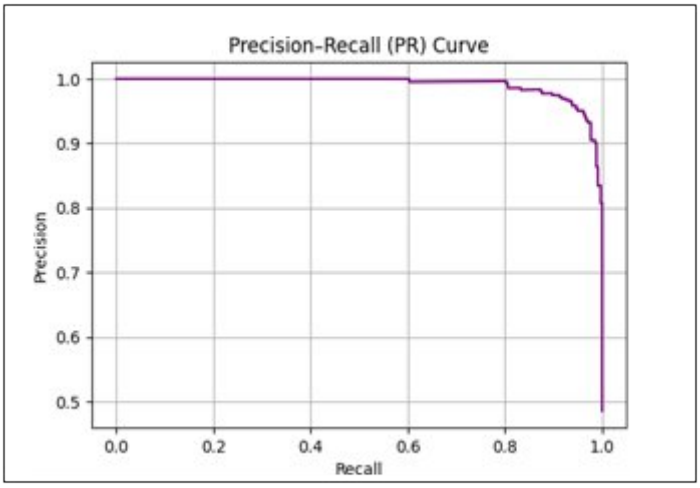

FIGURE 2: PR Curve

Precision–Recall (PR) curve maintains consistently high precision across a wide range of recall values, highlighting the robustness and stability of the model even under ammunition imbalance.

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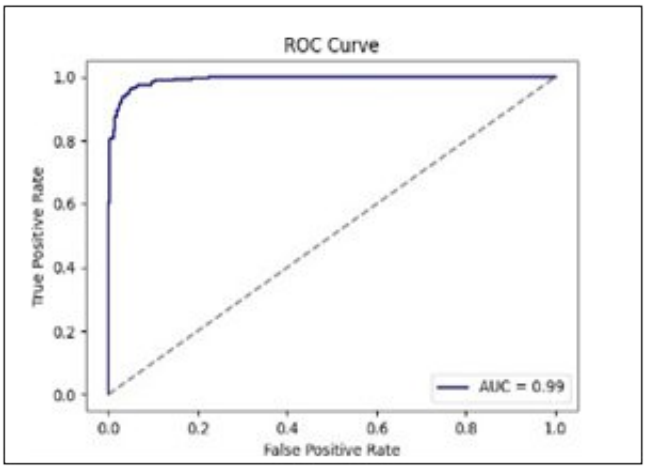

FIGURE 3: ROC Curve

This shows an impressive AUC reckoning of 0.99, indicating strong discriminative capability and minimal false-positive rate.

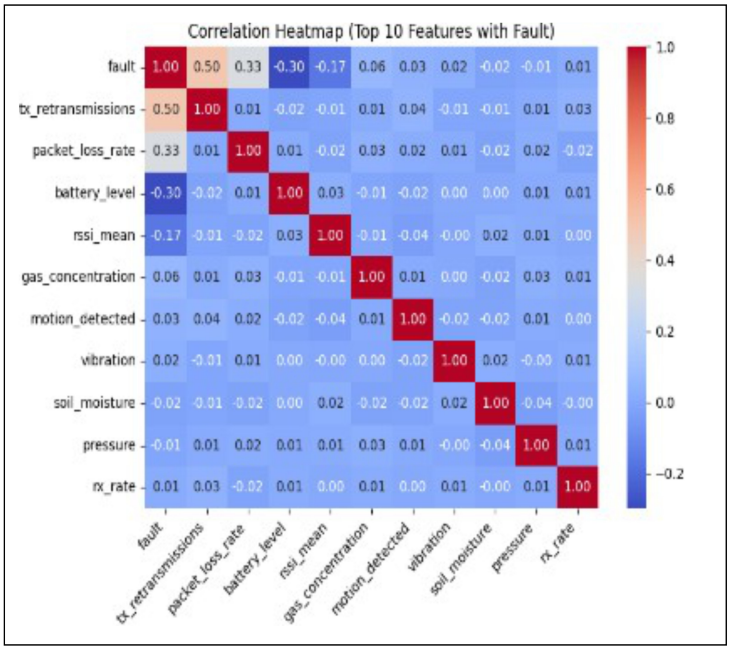

FIGURE 4: Correlation Heat Map

Each node measures and records vital readings such as battery level, temperature, humidity, CO_2 concentration, signal strength, packet loss rate, and network load.

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MODULE 1- Dataset Loading

```
--- Loading Dataset ---
      scenario  battery_level  ...  gas_concentration  fault
0        rural       0.477054  ...         245.468018      1
1        rural       0.191551  ...         246.331863      0
2        urban       0.124913  ...         260.097229      0
3        urban       0.380316  ...         171.864152      0
4   industrial       0.156267  ...         271.863225      1
5        rural       0.019819  ...         174.388967      0
6        urban       0.118730  ...         237.448486      1
7        rural       0.526994  ...         248.615237      1
8        urban       0.112416  ...         224.745460      1
9        rural       0.150426  ...         293.437153      1
10       urban       0.527769  ...         288.424441      1
11       rural       0.177550  ...         164.711345      0
12       urban       0.348049  ...         189.246922      0
13  industrial       0.195580  ...         320.157808      1
14       urban       0.176870  ...         318.527567      1
15  industrial       0.117443  ...         249.435225      1
16       urban       0.325833  ...         232.119962      1
17  industrial       0.213529  ...         247.644716      1
18       rural       0.369865  ...         238.046539      0
19       urban       0.281215  ...         262.135182      0
20       urban       0.199116  ...         327.029479      1
21       urban       0.288223  ...         263.022087      0
22  industrial       0.203703  ...         273.336570      1
23       urban       0.161252  ...         303.864231      1
24       rural       0.073338  ...         257.492058      1
25       urban       0.323058  ...         226.230798      1
26       urban       0.049349  ...         322.783393      1
27  industrial       0.467033  ...         277.020371      1
28       rural       0.252955  ...         330.069523      1
29       rural       0.579040  ...         163.167572      0

[30 rows x 22 columns]

Dataset shape: (3500, 22)
```

MODULE 2 - Transformation & Normalization

```
--- Preprocessing ---
Missing values: 0

Encoded categorical columns: ['scenario']

Class distribution before balancing:
fault
0    1800
1    1700
Name: count, dtype: int64

--- Building Hybrid Model ---
Model training complete.
```

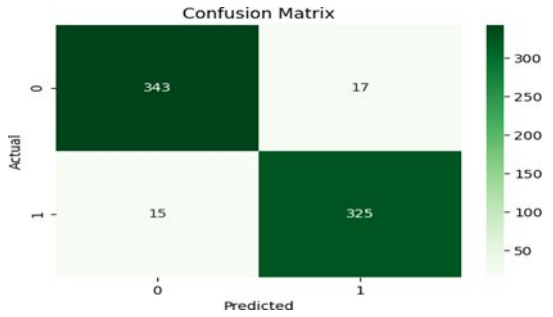

FIGURE 5: CONFUSION MATRIX

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The model correctly classified 343 normal instances (True Negatives) and 325 faulty instances (Positives), by mispredicting 17 samples as faults (False Positives) and 15 faulty samples as normal (False Negatives).

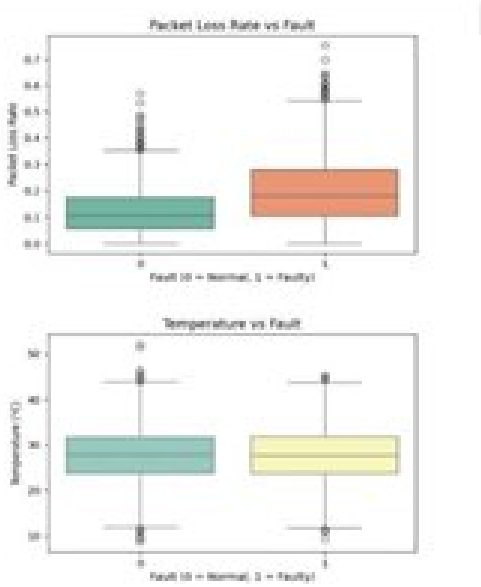

FIGURE 6: a) Packet Loss Rate Vs Fault b) Temperature Vs Fault

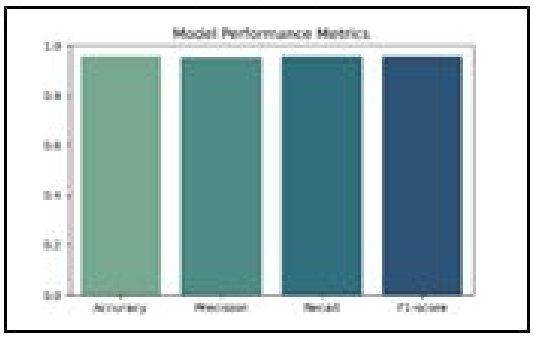

FIGURE 7: Graphical Parametric Comparison

As observed from the evaluation results, the model achieved an overall accuracy of 95.4%, confirming its strong predictive capability and generalization efficiency

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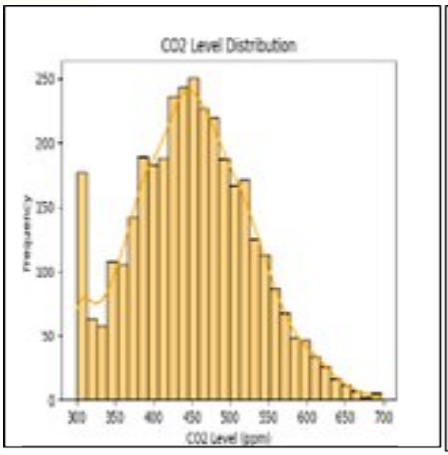

FIGURE 8: CO2 Level

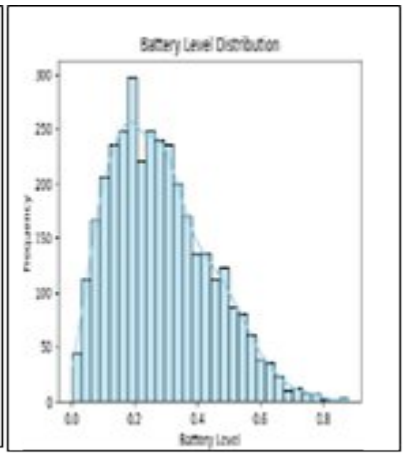

FIGURE 9: Battery Level Distribution

Distribution Process not only achieves high predictive accuracy but also provides transparent, interpretable insights into how different sensor and network parameters influence fault detection.

IV. SYSTEM ARCHITECTURE

The system operates in several sequential stages, begins with data preprocessing, where missing or duplicate records are removed, and categorical attributes are encoded using Label Encoding.

All numerical features are then normalized using a Standard Scaler to maintain uniformity in the data. To handle class imbalance between normal and faulty data, Synthetic Minority Over-sampling Technique is planned as an equilibrium training architype. Next, a Hybrid Machine Learning Model is constructed using three algorithms. These models are integrated using a soft-(XC9572XL) module, which drives an LED- based indicator—green for normal operation and red for a fault condition. Features are then normalized using a Standard Scaler to maintain uniformity in the data. Additionally, SHAP-based peculiarize deeper interpretability. Memory Elements are used to store intermediate values in sequential logic circuits, such as counters or shift registers. An electronic chip called a Universal Asynchronous Receiver/Transmitter that actually does the conversion and convert each byte to a stream of 1's and 0's and in reverse. Internal architecture of XC9572XL consists of Global Buffers which is used to distribute signals across the device, ensuring that timing and signal integrity are maintained across the entire chip.RS232 specification governs physical and electrical characteristics of serial communication and several additional signals that are asserted (set to logical 1) for information and control beyond the data signal.XC9572XL is programmed using JTAG, which allows for reconfiguration of the device via an external programming tool. Once programmed, the device logic is hardwired and performs desired function until reprogrammed. Device is configured by loading a bitstream file into device's non-volatile memory. In this paper all characters expressed as one byte. Bitstream defines how the logic block interconnects are configured. Half duplex serial communication needs at minimum two wires, signal ground and data line. Full duplex serial communication needs at minimum three wires, signal ground, transmit data line and receive data line. Device architecture based on a combination of logic gates, flip-flops and multiplexers is laid out using a hardware description language

Logic Blocks are the fundamental building units of the device. They can implement AND, OR, XOR, and other logical operations. Logic functions are based on the design requirements. Flip-Flops are used for storing state information and can be configured to work as registers, latches or memory elements. TXC9572XL uses programmable interconnects to connect the logic blocks in desired pattern forming a custom circuit. Baud rate signal switch states in one second. These signals are Carrier Detect Signal, Ring Indicator (RI), Data Set Ready (DSR), Clear To Send (CTS) all are asserted by modems to signal a successful connection to other modem, to signal the phone ringing, to show their presence, scan receive data. Data Terminal Ready (DTR), Request To Send (RTS) are assigned by terminals, show their presence and if they can receive data.RS232 Cabling describes signal connection. Fault-detection system integrates sensing nodes, a communication gateway, Python-based analysis and hardware indicators to provide a complete real-time monitoring

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solution. In this design, WSN nodes collect environmental or system data and transmit it wirelessly to a gateway implemented using an ESP32 module. ESP32 receives these packets through its communication interface and immediately forwards sensor information to a Python host computer using TTL-level UART communication.

V. MEASUREMENT RESULTS

As observed from the evaluation results, fortified an overall accuracy of 95.4%, by prefiguring the model effectively. This ensemble strategy successfully combines strength, enhancing both sensitivity and specificity precision for normal operation (0.9581) and fault detection (0.9503) signifies a high confidence in predictions, while recall values (0.9528 for normal and 0.9559 for fault) show that the model successfully identifies the majority of true cases in each category. The F1-scores of 0.9554 (normal) and 0.9531 (faulty) highlight the model's robustness in handling imbalanced data and maintaining consistent performance across both classes. Moreover, 0.9917 reflects effectiveness of the entirety architecture.

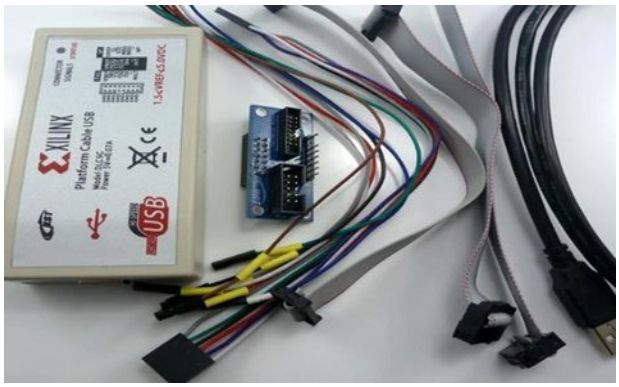

FIGURE 10: XILINX FLAH BLAST programmer

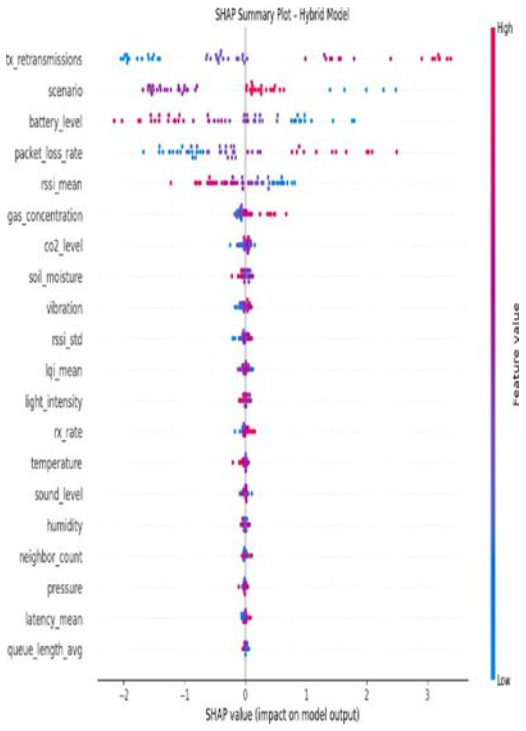

FIGURE11. SHAP Analysis

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Reveals that tx_retransmissions, scenario type, battery_level, packet_loss_rate, and rssi_mean are most influential driving model's decision.

The SHAP summary plot provides interpretation of the hybrid predictions by quantifying each feature to the fault classification. Python script acts as the core processing engine, it continuously reads incoming packet, validates data, checks node activity, evaluates sensor thresholds and identifies abnormal behaviour such as missing packets, out-of-range values. Based on the computed logic, it classifies the status of the network, then sends a simple fault flag back through the same TTL interface to the ESP32 and simultaneously to FPGA board. After decision is made, Python program sends a simple fault flag back through the same TTL interface to the ESP32 and simultaneously to an FPGA board. ESP32 uses this feedback to update an I²C-based LCD display, typically a 16x2 character module, showing either "SYSTEM NORMAL" or "FAULT DETECTED," along with optional sensor information. This real-time display allows local users to visually confirm the health of the WSN without accessing the computer.

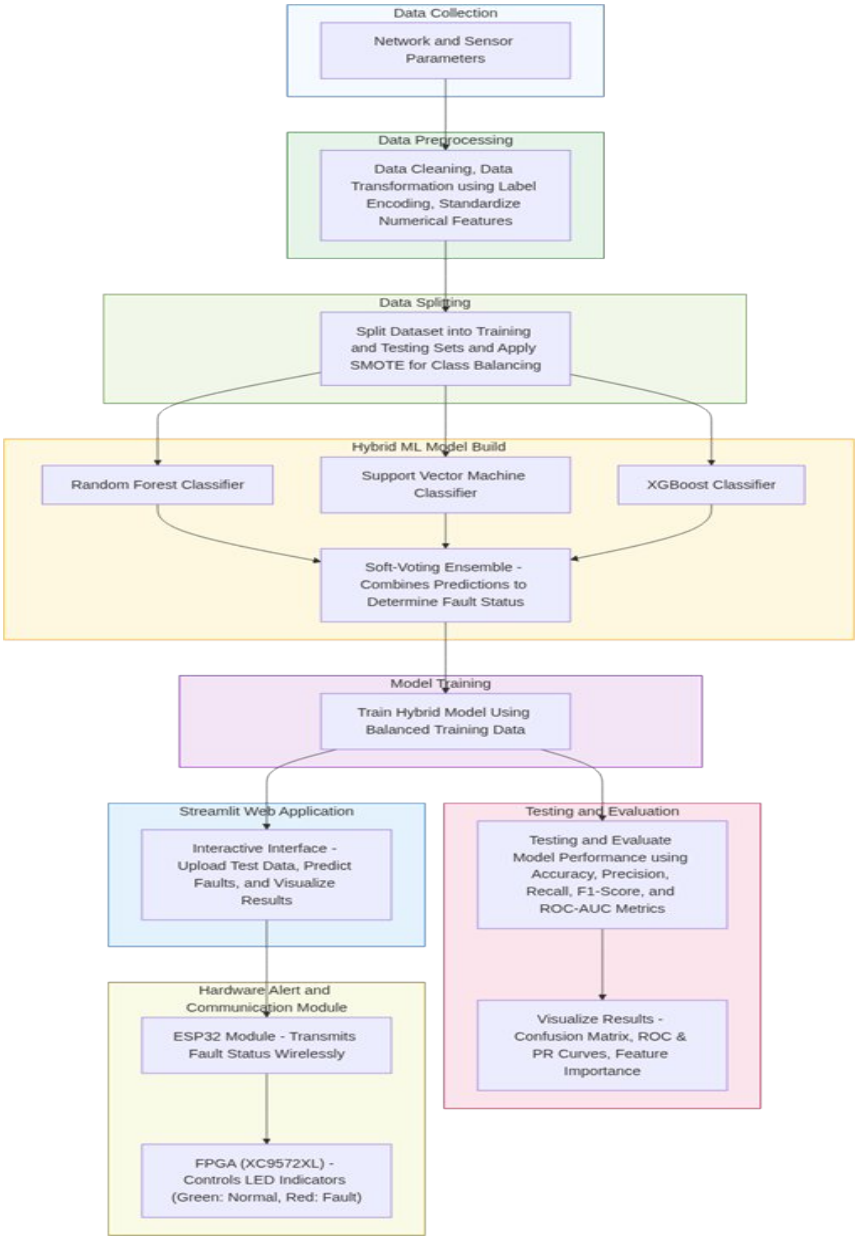

FIGURE 12: FLOW CHART

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This module simplifies testing and makes the system user-friendly for researchers and network engineers.

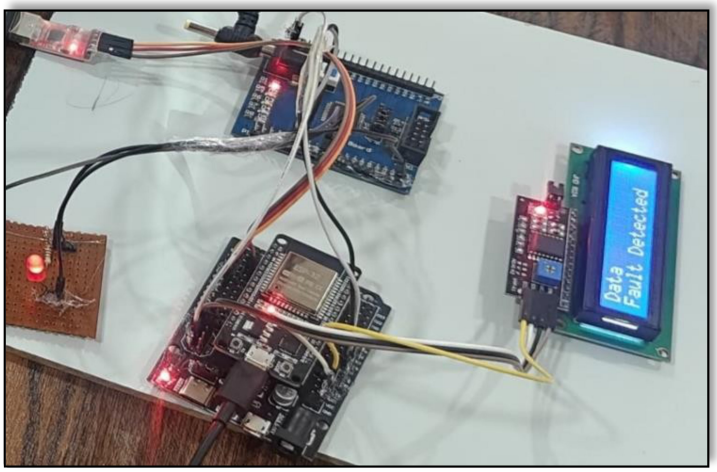

FIGURE13. The complete Hardware Part

System included with FPGA, ESP 32, LED, False Alarm Detector analyses the fault.

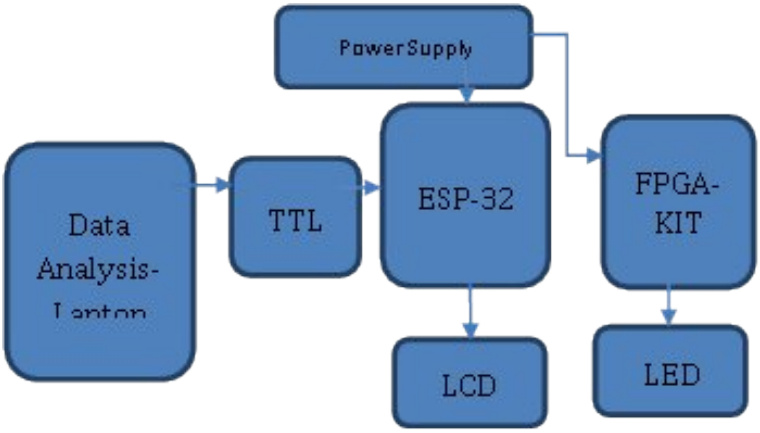

FIGURE14. Hardware Block Diagram

In parallel, FPGA receives a binary signal representing the fault status. When no fault is detected, the FPGA activates green LED, indicating normal operation; when a fault is present, FPGA lights the red LED, providing a simple but robust hardware-level alert. Through this layered architecture WSN sensing, ESP32 communication and display, Python-based fault analysis, and FPGA-driven LED indicators system delivers reliable end-to-end monitoring clear and immediate hardware outputs. ESP32 (30-pin) development board is a popular microcontroller based upon ESP32-WROOM-32 module.

Below are the details of its 30 pins, including power, GPIO, ADC, DAC, PWM, I2C, SPI, UART, and special function pins.

ESP32 30-Pin Development Board Pinout
Power Pins: VIN (V5) – 5V input from USB or external source
3V3 – 3.3V regulated output (used for powering sensors and modules) GND – Ground
General Purpose Input/Output
GPIO0 – Boot mode selection (must be LOW for programming) GPIO1 (TX0), GPIO3 (RX0) – UART0 for

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communication (USB serial)
GPIO2 – Connected to onboard LED Analog Input (ADC - 12-bit Resolution):
ADC1: GPIO36, GPIO39, GPIO34, GPIO35, GPIO32, GPIO33 ADC2: GPIO25, GPIO26, GPIO27, GPIO14, GPIO12
DAC (Digital to Analog Converter) Pins: DAC1: GPIO25, DAC2: GPIO26
I2C (Inter-Integrated Circuit) Pins:
(Default but can be changed in code) SDA (Data): GPIO21
SCL (Clock): GPIO22
UART (Serial Communication) Pins:
UART0 (Default Serial): TX(GPIO1), RX(GPIO3) UART1: TX(GPIO10), RX(GPIO9)
UART2: TX(GPIO17), RX(GPIO16)
PWM (Pulse Width Modulation) Pins:

Almost all GPIO pins can be used as PWM output.
Touch Sensor Pins: GPIO4, GPIO0, GPIO2, GPIO15, GPIO13, GPIO12, GPIO14, GPIO27, GPIO33, GPIO32
Hall Effect Sensor: Built-in (uses internal circuitry). A typical XC9572XL development board includes the main CPLD chip, a 10–12 MHz clock oscillator, a JTAG programming interface, several LED indicators, and push buttons for user input. It also has expansion headers for connecting external modules and a voltage regulator to provide stable 3.3V operation from a 5V USB or adapter supply. The board can be easily programmed using Xilinx ISE Design Suite through a USB JTAG cable, which loads ajed (JEDEC) configuration file into the CPLD. This board is ideal for learning and implementing basic digital circuits such as counters, multiplexers, decoders, sequence detectors, and finite state machines. It can also serve as a glue logic device interfacing microcontrollers or sensors with other digital components. XC9572XL is known for its low power consumption, fast switching speed and compact size making it suitable for embedded and educational applications compared to FPGA, it offers low complexity, instant startup and greater reliability for small logic functions.
Overall, XC9572XL provides an excellent platform for students, researchers and engineers to design, test, implement custom digital logic systems.

Signal ground data lines are connected in a null modem communication cable.
The two connector pins of the RS232 port, is used for flow control. These pins request RTS to send and CTS clear to send. DTE/DCE, a computer communicating with a modem device RTS is an output on the DTE and input on the DCE. CTS are the answering signal coming from the DCE.

16x2 Liquid Crystal Display, which means 16 characters per line is used.

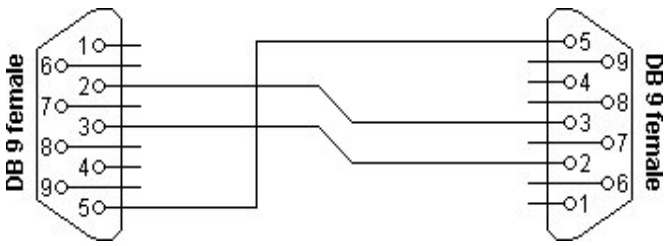

FIGURE15. NULL MODEM WITHOUT HANDSHAKING

HD44780U refers to the controller chip it receives data from an Atmega16 and communicates directly with the LCD. 8-bit mode of LCD is used as 8-bit data bus.

The three control lines are EN, RS, and RW. EN line is called "Enable" it indicates LCD that we are sending data. For sending data to LCD, the program make sure that the line is low (0) and then set the other two control lines on the data bus. When the other lines are ready, bring EN high (1) and wait for the minimum time required by the LCD datasheet and end by bringing it low again. If "Register Select" line is 0, the data is treated as a command instruction such as clear screen, position cursor, etc. When the RS is high (1), the data sent is displayed as text data. For example, to display the letter "B" on the screen you would set RS high. The RW line is “Read/Write" control line. When it is low,

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the information on the data bus is written to the LCD. When RW is high, the program questions the LCD." Get LCD status" is read command. All the others are write command, so RW will always be low. In case of an 8-bit data bus, the lines are referred to as DB0, DB1, DB2, DB3, DB4, DB5, DB6, and DB7.

Table 2 LCD Pin Description

Pin no	Name	Description
1	VSS	GND
2	VCC	Power supply (+5v)
3	VEE	Contrast Adjust
4	RS	0=Instruction Input 1=Data Input
5	R/W	0=Write to LCD 1=Read From LCD
6	EN	Enable Signal
7	D0	Bit 0 LSB
8	D1	Bit 1
9	D2	Bit 2
10	D3	Bit 3
11	D4	Bit 4
12	D5	Bit 5
13	D6	Bit 6
14	D7	Bit 7 MSB

CPLD Development kit is based on Xilinx XC9572XL is a low cost platform for training, testing and developing designs based on the Xilinx 9500XL family of CPLD. All user I/O pins are brought out of the 9572XL device. On-board power supply includes 3.3V regulator it regulates Vcc internal and I/O for the CPLD which is connected to Burgstick provided. JTAG programmer can be used for programming the XC9572XL. 40 MHz Crystal Oscillator provides clock source that is directly connected to GCK1 clock input on the 9572XL. HDL code can be implemented using Xilinx Website.

Xilinx XC9572XL is part of the Cool Runner-II family of programmable logic devices (PLDs). It is a CPLD (Complex Programmable Logic Device) designed to offer flexible, cost-effective solution for implementing custom logic in a variety of applications such as communication systems, automotive electronics, and industrial control systems. Xilinx JTAG Programming is a method used to configure and program Xilinx devices including Field-Programmable Gate Arrays, electrical characteristics, such as voltage levels can interface other

Complex Programmable Logic Devices, System on Chips, through a devices via these I/O pins, making it versatile for various applications.

Joint Test Action Group programming utilizes the IEEE 1149.1 standard and enables users to program devices by directly communicating with internal registers and memory cells through a dedicated JTAG port. Device designed to offer a flexible, cost-effective solution for implementing custom logic in automotive electronics, communication and industrial control systems. The board contains the 1600 gate, 72 macro cells, 100 Pin XC9572XL CPLD with 72 user I/O's.

The user first designs their logic or circuit using a HDL. Once design is complete, it is synthesized, optimized, and mapped into aconfigurationbitstream using Xilinx's tools (Vivado, ISE). Programming the Device: After synthesizing the design into a bitstream the file is sent to the target device via JTAG, it's programmer sends the bitstream through a series of data registers and memory cells in the target device. These registers are part of the device's configuration logic, and the bitstream defines the programmable logic set up. After programming, the JTAG interface allows for a quick verification process to ensure that the bitstream was correctly loaded and that the device operates as expected. JTAG tool can perform.

V. CONCLUSION

Developed model altogether attained 95.4% fidelity, showing its robustness and high predictive capability in distinguishing between normal and faulty sensor nodes. Assimilations including label encoding, feature standardization, and SMOTE balancing further improved model stability and performance. Streamlit-based web application was

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implemented to provide an intuitive interface for testing and visualization allowing users to upload data and view real-time prediction outcomes. Furthermore, the fault detection results were successfully interfaced with the FPGA (XC9572XL) and ESP32 modules, enabling hardware-level LED alerts for instant fault indication. Overall, the system offers a comprehensive and practical solution for intelligent fault detection and alerting in WSN environments, contributing to improved network reliability and operational efficiency.

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